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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Trung T. Doan et al.

Serial No.: 10/774,762

Filed: February 9, 2004

For: APPROACH TO AVOID BUCKLING
BPSG BY AN INTERMEDIATE
BARRIER LAYER

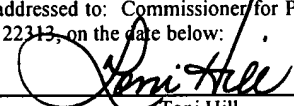
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Group Art Unit: 2822

Examiner: Novacek, Christy L.

Atty. Docket: MCRO:144-3/FLE
92-0321.04

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Date	Toni Hill

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on June 19, 2006, and received by the Patent Office on June 23, 2006, and in furtherance to the Panel decision mailed on July 25, 2006.

1. **REAL PARTY IN INTEREST**

The real party in interest is Micron Semiconductor, Inc., the Assignee of the above-referenced application by virtue of the Assignment recorded at reel 6574, frame 0073, and dated January 24, 1994.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any related appeals or interferences. The undersigned is Appellants' legal representative in this Appeal. Micron Semiconductor, Inc., the Assignee of the above-referenced application, as evidenced by the documents mentioned above, will be directly affected by the Board's decision in the pending appeal.

3. **STATUS OF CLAIMS**

Claims 19-42 are currently pending and under final rejection and, thus, are the subject of this appeal.

4. **STATUS OF AMENDMENTS**

The present application is not subject to any pending amendments.

5. **SUMMARY OF CLAIMED SUBJECT MATTER**

The present application currently contains four independent claims that are subject to this appeal, claims 19, 26, 33, and 39. To explain the subject matter defined by independent claims 19, 26, 33, and 39, specific exemplary embodiments are identified in the specification. However, it is important to note that the embodiments subsequently discussed merely explain subject matter, rather than defining the scope of the claims themselves. Thus, while the following embodiments are exemplary of claims 19, 26, 33, and 39, they are not definitive.

Independent claim 19, the first of the four independent claims subject to the present appeal, recites:

A semiconductor device substantially impervious to the effects of buckling, said device comprising:

- a) a single first planarization layer disposed on a semiconductor substrate, the single first planarization layer having a first reflow temperature and a first thermal coefficient of expansion;
- b) a barrier film disposed on the single first planarization layer; and
- c) a single second planarization layer disposed on the barrier film, the single second planarization layer having a second reflow temperature and a second thermal coefficient of expansion, wherein the barrier film does not reflow at the first or second reflow temperatures and retains its structural integrity to isolate the single first planarization layer from the single second planarization layer, thereby preventing the single first planarization layer and the single second planarization layer from interacting, and enabling the single first planarization layer and the single second planarization layer to uniformly reflow.

The semiconductor device of claim 19 is exemplified by a semiconductor device depicted by FIGS. 4-6 and described in the Specification. *See* Application, p. 8, l. 3-p. 10, l. 21. The exemplary semiconductor device includes a single first planarization layer 30 disposed on a substrate. *See* Application, p. 8, ll. 3-10; FIG. 4. In this embodiment, a barrier film 40 is disposed on the single first planarization layer 30. *See* Application, p. 8, l. 11-p. 9, l. 16; FIG. 5. Further, in the embodiment of FIGS. 4-6, a second single planarization layer 50 is disposed on the barrier film 40. *See* Application, p. 9, l. 17-p. 10, l. 21. As explained in the Specification on page 10, lines 5-20, the barrier film 40 does not reflow at the reflow temperatures of the other

layers 30 and 50, and it retains its structural integrity to isolate the single first planarization layer 30 from the single second planarization layer 50. Thus, in this embodiment, the barrier film 40 prevents the single first planarization layer 30 and the single second planarization layer 50 from interacting and enables the single first planarization layer 30 and the single second planarization layer 50 to reflow uniformly. *See Application*, p. 10, ll. 14-20.

Turning to the second independent claim subject to the present appeal, independent claim 26 recites:

A planar multilayered semiconductor device comprising:
a substrate;
a first single flowable layer disposed on the substrate and having a thermal coefficient of expansion;
a nitride film disposed on the first layer; and
a second single flowable layer disposed on the nitride film, the second single flowable layer having another thermal coefficient of expansion, wherein the nitride film retains its structural integrity at the reflow temperatures of the first single flowable layer and the second single flowable layer, thereby preventing the first single flowable layer and the second single flowable layer from interacting, and enabling the first single flowable layer and the second single flowable layer to uniformly reflow.

As with the previous claim, independent claim 26 is explained by referring to an exemplary embodiment described in the Specification. The semiconductor device of claim 26 is exemplified by the semiconductor device depicted by FIGS. 4-6. *See Application*, p. 8, l. 3-p. 10, l. 21; FIG. 6. The exemplary semiconductor device includes a single first flowable layer 30 disposed on a substrate. *See Application*, p. 8, ll. 3-10; FIG. 4. In this embodiment, a nitride film 40 is disposed on the single first flowable layer 30. *See Application*, p. 8, l. 11-p. 9, l. 16;

FIG. 5. Further, in the embodiment of FIGS. 4-6, a second single flowable layer 50 is disposed on the nitride film 40. *See Application*, p. 9, l. 17-p. 10, l. 21. As explained in the Specification on page 10, lines 5-20, the nitride film 40 does not reflow at the reflow temperatures of the other layers 30 and 50, and it retains its structural integrity to isolate the single first flowable layer 30 from the single second flowable layer 50. Thus, in this embodiment, the nitride film 40 prevents the single first flowable layer 30 and the single second flowable layer 50 from interacting and enables the single first flowable layer 30 and the single second flowable layer 50 to reflow uniformly. *See Application*, p. 10, ll. 14-20.

Turning to the third independent claim subject to the present appeal, independent claim 33 recites:

A multilayer heterostructure semiconductor device having a planar configuration comprising:
a semiconductor substrate;
a first single planarization layer disposed on the substrate, the single first planarization layer having a first thermal coefficient of expansion and a first reflow temperature;
a barrier film disposed on the single planarization layer, said barrier film having structural integrity; and
a single second layer disposed on the barrier film, wherein the barrier film prevents the single first planarization layer and the single second layer from interacting when the single first planarization layer is heated to a temperature above the first reflow temperature, the single second layer having a second thermal coefficient of expansion.

Independent claim 33 is explained by referring to an exemplary embodiment described in the Specification. The semiconductor device of claim 33 is also exemplified by the semiconductor device depicted by FIGS. 4-6. *See Application*, p. 8, l. 3-p. 10, l. 21; FIG. 6. The

exemplary semiconductor device includes a first single planarization layer 30 disposed on a substrate. *See* Application, p. 8, ll. 3-10; FIG. 4. In this embodiment, a barrier film 40 is disposed on the first single planarization layer 30. *See* Application, p. 8, l. 11-p. 9, l. 16; FIG. 5. Further, in the embodiment of FIGS. 4-6, a single second layer 50 is disposed on the barrier film 40. *See* Application, p. 9, l. 17-p. 10, l. 21.

Turning to the fourth independent claim subject to the present appeal, independent claim 39 recites:

An apparatus, comprising:
a first layer at a temperature of at least 700°C, the first layer being in a reflow state;
a second layer at the temperature of at least 700°C, the second layer being in a reflow state;
a barrier layer at a temperature of at least 700°C, the barrier layer being disposed between the first and second layers, wherein the barrier layer is not in a reflow state and maintains its structural integrity to isolate the first layer from the second layer.

As with the previous claims, independent claim 39 is explained by referring to an exemplary embodiment described in the specification. The semiconductor device of claim 39 is also exemplified by the semiconductor device depicted by FIGS. 4-6. *See* Application, p. 8, l. 3-p. 10, l. 21; FIG. 6. The exemplary semiconductor device includes a first layer 30, a second layer 50, and a barrier layer 40. *See id.* In this embodiment, the layers 30, 40, and 50 are at 700°C, and the barrier layer 40 is not in a reflow state. *See* Application, p. 10, ll. 5-20.

6. **GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

Rejection of Claims 19-38 under 35 U.S.C. § 102

Appellants respectfully urge the Board to review and reverse the Examiner's rejection of claims 19-38 under 35 U.S.C. § 102 as being anticipated by Woo et al. (U.S. Patent No. 5,262,352, hereinafter "Woo").

Rejection of Claims 39-42 under 35 U.S.C. § 103

Appellants respectfully urge the Board to review and reverse the Examiner's rejection of claims 39-42 under 35 U.S.C. § 103 as being rendered obvious by Woo in view of Cheung et al. (U.S. Patent No. 4,693,925, hereinafter "Cheung").

7. **ARGUMENT**

As discussed in detail below, the Examiner has improperly rejected the pending claims. The Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Section 102 and Section 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants respectfully assert that claims 19-42 are currently in condition for allowance.

Rejection of Claims 19-38 under 35 U.S.C. § 102

In the Final Office Action Mailed June 17, 2006, the Examiner rejected claims 19-38 under 35 U.S.C. § 102 as being anticipated by Woo. Specifically, the Examiner stated:

Regarding claims 19 and 27, Woo discloses a single first planarization layer (14 and/or 15) disposed on a semiconductor substrate (10), a barrier film (16) having a structural integrity disposed on the first

planarization layer, a single second planarization layer (17 and/or 18 and/or 20) disposed on the barrier film (col. 3, ln. 22 - col. 4, ln. 15). Inherently, the first and second planarization layers have reflow temperatures and thermal coefficients of expansion. Woo does not specifically disclose that the second layer is isolated from the first layer when a temperature of 700°C or greater is applied. However, because the first layer, barrier layer, and second layer are made of the same materials as those of Applicant's invention, it appears that the layered structure of Woo would inherently possess the function of the second layer is isolated from the first layer when a temperature of 700°C or greater is applied. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on"; and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103). Additionally, it is noted that claims 19-38 are product claims. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

...

Regarding claims 26, 28 and 37, Woo discloses a first single layer (14 and/or 15), inherently having a

thermal coefficient of expansion, a nitride film (16) superjacent the first layer, and a second single layer (17 and/or 18 and/or 20), inherently having another thermal coefficient of expansion, superjacent the nitride film (col. 3, ln. 22 - col. 4, ln. 15). Woo does not specifically disclose that the first and second layers are flowable at temperatures of at least 700°C. However, because the first and second layers are made of the same materials as those of Applicant's invention, it appears that these layers of Woo would inherently possess the function of being flowable. *See In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on");

...

Regarding claim 33, Woo discloses a semiconductor substrate (10), a first single planarization layer (14 and/or 15), inherently having a thermal coefficient of expansion and a first reflow temperature, on the substrate, a barrier film (16) having structural integrity on the planarization layer, and a second single layer (17 and/or 18 and/or 20), inherently having a thermal coefficient of expansion, superjacent the barrier film (col. 3, ln. 22 - col. 4, ln. 15). Woo does not specifically disclose that the barrier film prevents the planarization layer and the second layer from interacting when heated. However, because the first layer, barrier layer, and second layer are made of the same materials as those of Applicant's invention, it appears that the layered structure of Woo would inherently possess the function of preventing the planarization layer and the "another layer" from interacting when heated. *See In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the

prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on").

Final Office Action Mailed March 17, 2006, pp. 2-5.

Appellants respectfully request reversal of this rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every limitation of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). The prior art reference also must show the *identical* invention "in as complete detail as contained in the ... claim" to support a *prima facie* case of anticipation. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989). Accordingly, Appellants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter.

Woo Does not Teach or Suggest Planarization Layers

The Examiner's rejection should be reversed for a number of reasons. The cited reference does not teach or suggest "a single first planarization layer" or "a single second planarization layer," as recited by independent claims 19 and 33. (Emphasis added.) In sharp contrast, the Woo reference teaches alternating dielectric layers 12, 16, and 20 and conductor layers 14 and 18. There is no evidence that any of these layers taught by the Woo reference

serve to planarize the film stack. Indeed, Appellants note that the Final Office Action does not cite any portion of the Woo reference that indicates any of these layers are actually planarization layers. Thus, the Woo reference does not teach all the features of claims 19 or 33 or the claims that depend therefrom.

In response to this point, the Examiner made two assertions, stating “Claims 19 and 33 do not recite that the first and second layers planarize the film stack. Additionally, Woo shows that the first and second layers are planar (see Figures 1-4).” Final Office Action Mailed March 17, 2006, p. 8.

The Examiner’s arguments fail to address the flaws in the rejection. In response to the Examiner’s first assertion that claims 19 and 33 do not recite that the first and second layers planarize the film stack, Appellants stress that the Examiner has misinterpreted the term “planarization layer.” Interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999). Here, the Examiner has asserted that one of skill in the art would not understand “planarization layer” to mean a layer that planarizes the film stack. The term “planarization” clearly modifies the word “layer.” Thus, the Examiner’s interpretation of “planarization layer” is inconsistent with the interpretation that those skilled in the art would reach. Indeed, one of ordinary skill in the art would not interpret the term “planarization layer” to refer to a layer that does not planarize an underlying non-planar layer.

With reference to the Examiner's second assertion that Figs. 1-4 of Woo show layers that are planar, Appellants stress that the Woo reference does not suggest that any of these layers is a "planarization layer." Layers 14, 15, 17, 18, and 20 are all formed upon a flat surface in the figures cited by the Examiner. Thus, none of these layers is positioned over topography that could be "planarized," and the fact that these layers may appear planar in Figs. 1-4 does not indicate that any of these layers is a "planarization layer" in the normal sense of the term, i.e., a layer that planarizes an underlying non-planar layer. Thus, Appellants reiterate that layers 14, 15, 17, 18, and 20 are not planarization layers.

In short, the Woo reference does not teach or suggest "a single first planarization layer" or "a single second planarization layer," as recited by independent claims 19 and 33. (Emphasis added.) For this reason among others, the Woo reference does not teach all the features of claims 19 or 33 or the claims that depend therefrom, and the rejection of these claims under Section 102 should be reversed.

Woo Does not Teach or Suggest Flowable Layers

Similarly, the Woo reference does not teach or suggest "a first single flowable layer" or "a second single flowable layer," as recited by independent claim 26. (Emphasis added.) Indeed, the Examiner has not cited any evidence that the layers disclosed by the Woo reference are flowable. In an attempt to locate a flowable layer in the Woo reference, the Examiner asserted that because the layers in the Woo reference "are made of the same materials as those of Applicant[s]" invention, it appears that these layers of Woo would inherently possess the function of being flowable." Final Office Action Mailed March 17, 2006, p. 4. However, as is well known in the

art, a layer is not flowable merely because it contains certain materials without regard to the particular composition of the compound, as well as other properties. *See e.g.* Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era Volume 1: Process Technology* 200 (Lattice Press 2000) (explaining that the capacity of borophosphosilicate glass to flow at a given temperature is a function of the *concentration* of boron and phosphorous in the glass); and *Id.* at 737 (indicating that *film thickness* governs the capacity of resist to planarize, i.e. flow from high points to low points). Notably, factors other than the mere presence of certain materials in a layer significantly contribute to the capacity of a layer to flow. Thus, contrary to the Examiner's assertion, the layers taught by the Woo reference are not inherently flowable. Therefore, the Woo reference does not disclose all the features of claim 26 or the claims that depend therefrom.

In response to this explanation, the Examiner asserted that:

Applicant has provided no evidence that the first and second layers taught by Woo are not inherently flowable. Furthermore, Applicant's specification does not state that the first and second layers have to formed in any particular way in order to be flowable. Also, Applicant argues "Silicon Processing for the VLSI Era Volume 1" allegedly explains that the capacity of BPSG to flow at a given temperature is a function of the concentration of dopants therein. However, Applicant has not provided this reference and none of the rejections of claims 19-42 state that layers of BPSG inherently flow at a given temperature.

Final Office Action Mailed March 17, 2006, p. 8.

Appellants did not include a copy of the cited portions of Silicon Processing for the VLSI Era in the previous response due to an oversight. However, with this Appeal Brief, a copy is provided in the attached appendix.

With regard to the Examiner's other arguments, Appellants strongly disagree. The cited portions of Silicon Processing for the VLSI Era are evidence that the Examiner's rationale for inherency is fundamentally flawed. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Here, the Examiner asserted that that because the layers in the Woo reference "are made of the same materials as those of Applicant[s'] invention, it appears that these layers of Woo would inherently possess the function of being flowable." Final Office Action Mailed March 17, 2006, p. 4. However, the cited portions of Silicon Processession for the VLSI Era demonstrate that a layer is not necessarily flowable because it is made of a given material without regard to other factors, such as relative concentration and thickness. Thus, the layers taught by the Woo reference are not inherently flowable, and the Woo reference does not teach or suggest "first single flowable layer" or "a second single flowable layer."

Accordingly, Appellants reiterate that the Woo reference does not disclose all the features of claim 26 or the claims that depend therefrom and request that the Board reverse the rejection of these claims under Section 102.

Woo Does not Teach or Suggest the Claimed Combinations of Layers

Finally, the Woo reference does not teach or suggest the combination of layers recited by independent claims 19, 26 or 33. The Woo reference depicts a film stack in Figure 1 and lists a large number of candidate materials for each layer in the film stack in columns 3 and 4. However, the Woo reference absolutely fails to disclose how to select among these candidate materials to produce the combination of layers recited by the present claims. For example, claim 19 recites a barrier film that “does not reflow at the first or second reflow temperatures” of the single first planarization layer and the single second planarization layer. In sharp contrast, the Woo reference does not teach how to combine the candidate materials listed for each layer in Figure 1 to produce such a relationship between the reflow temperatures of a barrier layer and planarization layers. Indeed, the Woo reference does not discuss the properties of “planarization” or “reflow” at all. Therefore, due to this lack of guidance as to how to select among the candidate materials for each layer, the Woo reference does not teach the combination of layers recited by claims 19, 26 or 33. Thus, for this reason also, the Woo reference cannot anticipate independent claims 19, 26 or 33. Appellants note that although Appellants identified this deficiency, the Examiner did not address this deficiency of the Woo reference in the Final Office Action Mailed March 17, 2006, as required by M.P.E.P. § 707.07(f).

For these reasons, Appellants respectfully request reversal of the rejections under 35 U.S.C. § 102 and allowance of claims 19-38.

Rejection of Claims 39-42 under 35 U.S.C. § 103

In the Final Office Action Mailed April 18, 2006, the Examiner rejected claims 39-42 as rendered obvious by Woo in view of Cheung. Specifically, the Examiner stated:

Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. (US 5,262,352) in view of Cheung et al. (US 4,693,925).

Regarding claim 39, Woo discloses a first layer (14 and/or 15), a second layer (17 and/or 18 and/or 20), and a barrier layer (16) in between the first and second layers (col. 3, ln. 22 - col. 4, ln. 15). Woo does not specifically disclose subjecting the first, second and barrier layers to a temperature of 700°C or greater. However, Woo does disclose depositing a polysilicon interconnection layer (24) and siliciding the polysilicon interconnection layer after the first, second and barrier layers have been formed (col. 5, ln. 26-27). Like Woo, Cheung discloses depositing a polysilicon interconnection layer and siliciding the polysilicon layer. Cheung teaches that the polysilicon can be successfully silicided by depositing a layer of refractory metal on the polysilicon layer and annealing the substrate at a temperature of 600-800°C (col. 5, ln. 44-50; col. 3, ln. 39-45). At the time of the invention, it would have been obvious to one of ordinary skill in the art to subject the first, second and barrier layers of Woo to an anneal of 700°C or greater because Woo discloses siliciding the polysilicon interconnection layer after the first, second and barrier layers have been formed and Cheung teaches that a polysilicon interconnection layer can be successfully silicided by subjecting the polysilicon and metal layer to an anneal of 600-800°C.

Woo does not specifically disclose that the barrier film prevents the planarization layer and the second layer from interacting when heated. However, because the first layer, barrier layer, and second layer are made of the same materials as those of Applicant's invention, it appears that the layered structure of Woo would inherently possess the function of preventing the planarization layer and

the "another layer" from interacting when heated. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on").

Final Office Action Mailed March 17, 2006, pp. 6-7.

Appellants respectfully request reversal of this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Features neither Taught nor Suggested by the Cited References or a Combination Thereof

The Woo reference and the Cheung reference, taken alone or in combination, fail to teach or suggest all the features of independent claim 39. For instance, the cited references do not disclose a first layer “in a reflow state,” as recited by claim 39. In contrast, the Woo reference does not disclose any layers in a reflow state, and the cited portion of the Cheung reference teaches a heat pulse of 600°C to 800°C for 10 to 20 seconds. The Chueng reference teaches that this heat pulse permits a “reaction to occur forming the metal silicide,” and not that any layer is in a reflow state. See Chueng, col. 3, ll. 45-50. In fact, the Examiner did not identify any layer in a reflow state in the Final Office Action. Thus, Appellants respectfully request withdrawal of this rejection and allowance of claim 39 and the claims that depend therefrom.

Consequently, the combination of the Woo reference and the Cheung reference cannot render claim 39 (or the claims depending therefrom) obvious. The Appellants respectfully assert that the rejection of claims 39-42 under Section 103 is erroneous and should be reversed and that claims 39-42 are allowable.

Conclusion


In view of the above remarks, Appellants respectfully submit that the Examiner has provided no supportable position or evidence that claims 19-38 are anticipated under Section 102 or that claims 39-42 are obvious under Section 103. Accordingly, Appellants respectfully request that the Board find claims 19-42 patentable over the prior art of record, reverse all outstanding rejections, and allow claims 19-42.

In accordance with 37 C.F.R. § 1.136, Appellants request that this and any future reply requiring an extension of time be treated according to the General Authorization For Extensions Of Time previously submitted.

The Commissioner is authorized to charge the requisite fee of \$500.00, and any additional fees which may be required, to the attached PTO-2038. However, if the PTO-2038 is missing, if the amount listed thereon is insufficient, or if the amount is unable to be charged to the credit card for any other reason, the Commissioner is authorized to charge Deposit Account No. 06-1315; Order No. MCRO:0144-3/FLE (02-1041,01).

Respectfully submitted,

Date: August 25, 2006



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8. **APPENDIX OF CLAIMS ON APPEAL**

1-18. (Cancelled)

19. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, said device comprising:

- a) a single first planarization layer disposed on a semiconductor substrate, the single first planarization layer having a first reflow temperature and a first thermal coefficient of expansion;
- b) a barrier film disposed on the single first planarization layer; and
- c) a single second planarization layer disposed on the barrier film, the single second planarization layer having a second reflow temperature and a second thermal coefficient of expansion, wherein the barrier film does not reflow at the first or second reflow temperatures and retains its structural integrity to isolate the single first planarization layer from the single second planarization layer, thereby preventing the single first planarization layer and the single second planarization layer from interacting, and enabling the single first planarization layer and the single second planarization layer to uniformly reflow.

20. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said barrier film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, tantalum oxide, silicon dioxide, silicon nitride and tetraethylorthosilicate ("TEOS").

21. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein the single first planarization layer comprises

at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass (“BPSG”) and tetraethylorthosilicate (“TEOS”).

22. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said single second planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass (“BPSG”) and tetraethylorthosilicate (“TEOS”).

23. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein the single second planarization layer comprises a metal.

24. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein the single second planarization layer comprises a refractive metal.

25. (Previously presented) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein the single second planarization layer comprises at least one of borophosphosilicate glass (“BPGS”) and tetraethylorthosilicate (“TEOS”).

26. (Previously presented) A planar multilayered semiconductor device comprising:

a substrate;

a first single flowable layer disposed on the substrate and having a thermal coefficient of expansion;

a nitride film disposed on the first layer; and

a second single flowable layer disposed on the nitride film, the second single flowable layer having another thermal coefficient of expansion, wherein the nitride film retains its structural integrity at the reflow temperatures of the first single flowable layer and the second single flowable layer, thereby preventing the first single flowable layer and the second single flowable layer from interacting, and enabling the first single flowable layer and the second single flowable layer to uniformly reflow.

27. (Previously presented) The planar multilayered semiconductor device according to claim 26, wherein said nitride film isolates the first single flowable layer from the second single flowable layer, thereby preventing the first single flowable layer and the second single flowable layer from interacting when heated.

28. (Previously presented) The planar multilayered semiconductor device according to claim 27, wherein the first single flowable layer and the second single flowable layer reflow at a temperature of at least 700°C.

29. (Previously presented) The planar multilayered semiconductor device according to claim 28, wherein said nitride film comprises at least one of titanium nitride, tantalum nitride, and silicon nitride.

30. (Previously presented) The planar multilayered semiconductor device according to claim 29, wherein the first single flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

31. (Previously presented) The planar multilayered semiconductor device according to claim 30, wherein the second single flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

32. (Previously presented) The planar multilayered semiconductor device according to claim 30, wherein the first single flowable layer comprises at least one of single crystal silicon, polycrystalline silicon, amorphous silicon.

33. (Previously presented) A multilayer heterostructure semiconductor device having a planar configuration comprising:

a semiconductor substrate;

a first single planarization layer disposed on the substrate, the single first planarization layer having a first thermal coefficient of expansion and a first reflow temperature;

a barrier film disposed on the single planarization layer, said barrier film having structural integrity; and

a single second layer disposed on the barrier film, wherein the barrier film prevents the single first planarization layer and the single second layer from interacting when the single first

planarization layer is heated to a temperature above the first reflow temperature, the single second layer having a second thermal coefficient of expansion.

34. (Previously presented) The multilayered heterostructure semiconductor device according to claim 33, wherein said barrier film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, silicon nitride, tantalum oxide, silicon dioxide, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

35. (Previously presented) The multilayered heterostructure semiconductor device according to claim 34, wherein said single first planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

36. (Previously presented) The multilayered heterostructure semiconductor device according to claim 35, wherein the single second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

37. (Previously presented) The multilayered heterostructure semiconductor device according to claim 33, wherein the single first planarization layer and the single second layer reflow at a temperature of at least 700°C.

38. (Previously presented) The multilayered heterostructure semiconductor device according to claim 37, wherein said structural integrity of said barrier layer is maintained when heated to a temperature of at least 700°C.

39. (Previously presented) An apparatus, comprising:
a first layer at a temperature of at least 700°C, the first layer being in a reflow state;
a second layer at the temperature of at least 700°C, the second layer being in a reflow state;
a barrier layer at a temperature of at least 700°C, the barrier layer being disposed between the first and second layers, wherein the barrier layer is not in a reflow state and maintains its structural integrity to isolate the first layer from the second layer.

40. (Previously presented) The apparatus of claim 39, wherein the first layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass (“BPSG”) and tetraethylorthosilicate (“TEOS”).

41. (Previously presented) The apparatus of claim 39, wherein the second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass (“BPSG”) and tetraethylorthosilicate (“TEOS”).

42. (Previously presented) The apparatus of claim 39, wherein the barrier layer comprises at least one of titanium nitride, tantalum nitride, titanium oxide, silicon nitride, tantalum oxide, silicon dioxide, borophosphosilicate glass (“BPSG”) and tetraethylorthosilicate (“TEOS”).

9. **EVIDENCE APPENDIX**

A copy of pages 200 and 737 of Silicon Processing fro the VLSI Era Volume 1: Process Technology is included herein. A copy of these pages was not provided prior to this Appeal Brief due to an oversight. However, the pages were cited and the relevant subject matter therein was paraphrased in the Response and Amendment filed on December 19, 2005 on page 12.

10. **RELATED PROCEEDINGS APPENDIX**

None

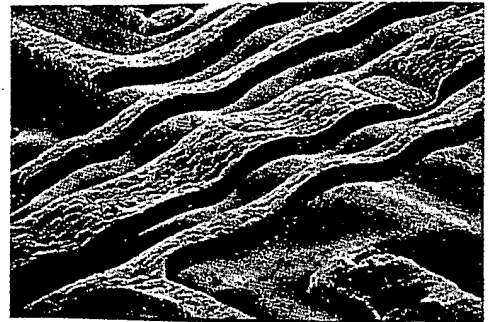
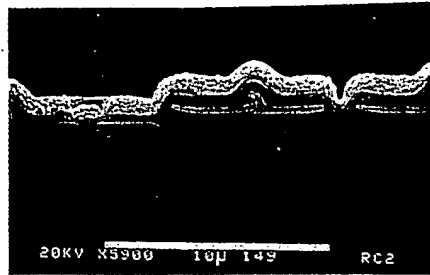


Fig. 6-42 Micrographs showing BPSG as the interlevel dielectric under the metal. Reprinted with permission of Semiconductor International.²

over abrupt steps in the substrate topography. Glass flow temperatures as low as 850°C can be obtained by adding boron dopant (e.g., B_2H_6) to the PSG gas flow to form the *ternary* (three component) oxide system B_2O_3 - P_2O_5 - SiO_2 , *borophosphosilicate glass*, or BPSG⁵⁹ (Fig. 6-42). Such films find wide use as the pre-metal dielectric layer between polysilicon and metal, and as dielectrics between stacked capacitors and metal in DRAMs. Even lower glass flow temperatures (i.e., 750°C) have been reported for BPSG films formed with TEOS/ O_3 .⁶¹

BPSG flow depends upon film composition, flow temperature, flow time, and flow ambient. It has been reported that an increase in boron concentration of 1 wt % in BPSG decreases the required flow temperature by ~40°C.⁵⁹ A plot of required flow temperatures versus BPSG dopant concentrations in LPCVD films is shown in Fig. 6-43. However, increasing the P concentration beyond ~5 wt % does not further decrease BPSG flow temperatures. An upper limit on boron concentration is also imposed by film stability. That is, BPSG films containing over 5 wt % boron tend to be very hygroscopic and unstable (second phase nucleation and precipitation of boric acid B_2O_3 and phosphoric acid P_2O_5 crystallites occurs, which can then lead to the formation of insoluble BPO_4 crystallites during the reflow process). Such precipitation is deleterious to film performance since the acid particles (though soluble) leave pits in the glass that are decorated later, and they leave local areas of low dopant concentration that affect the flow performance of the glass. The BPO_4 particles remain behind as defects.

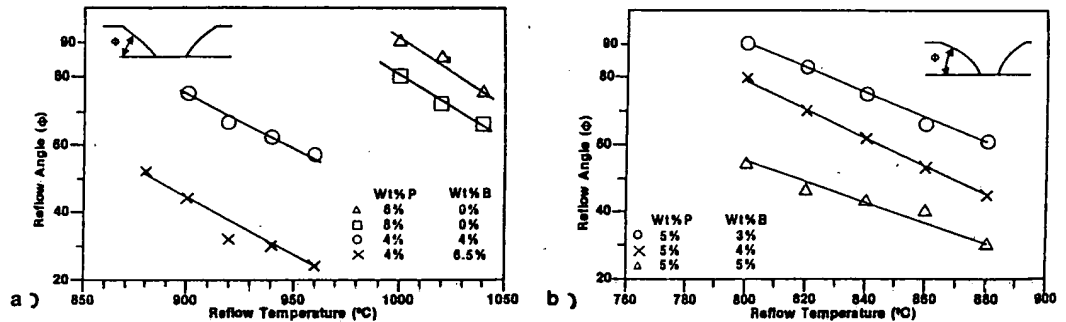


Fig. 6-43 (a) Reflow angle vs. reflow temperatures in a nitrogen ambient (30 min). (b) Reflow angle versus reflow temperatures in a steam ambient (30 min). Reprinted by permission of Solid State Technology, published by PennWell.⁶⁰

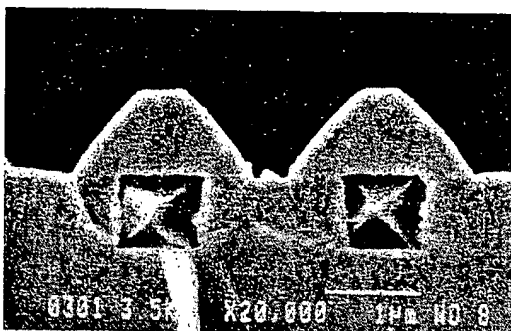


Fig. 15-12 At the conclusion of a CVD/Etch process, the surface topography over narrow lines will have a pyramid structure.¹⁶ (© 1987 IEEE).

wiring technology with metal pitches of $1.9 \mu\text{m}$ for Metal-1 and $2.4 \mu\text{m}$ for Metal-2 that uses this method to form the interlevel dielectric.¹⁸

There are three main drawbacks to this multiple CVD/Etch process: 1) the throughput is very low, even when batch CVD and etch reactors are used; 2) an erosion step must be used to planarize the pyramid structures over narrow lines (further reducing throughput); and 3) global planarization is not achieved (i.e., complete planarization is not achieved over wide steps).

15.3.3 Planarization through Sacrificial-Layer Etchback

Planarization of CVD interlevel-dielectric films can also be achieved using the *sacrificial-layer etchback technique* (Fig. 15-13). This method gained the most widespread acceptance in two-level-metal processes down to $\sim 1 \mu\text{m}$ device technologies (and even in some reported three-level-metal bipolar processes). Using this approach, it is possible to achieve a high degree of planarization between steps that are $\sim 2\text{--}10 \mu\text{m}$ apart. With more closely spaced features, the technique runs into problems. For more widely spaced steps, planarization is less complete. The process is carried out by first depositing the CVD film that will serve as the PMD or IMD. This layer is then coated with a film that will later be etched off (sacrificed). In most cases, such sacrificial layers are photoresists, spun on in liquid form. Upon being baked, these liquids become solid thin films that are thick enough so they provide a film surface that is close to being flat, as shown in Fig. 15-14. As long as the feature size is smaller than $10 \mu\text{m}$, the degree of planarization can exceed 70% with most photoresists.

In the next step, the sacrificial layer is first rapidly etched back in a plasma (typically, O_2 or O_2 mixed with CF_4) until the topmost regions of the dielectric layer are just exposed (Fig. 15-13b). The etch chemistry is then modified so the sacrificial-layer material and the dielectric are etched at approximately the same rate. The etch is continued under these conditions until all of the sacrificial layer has been etched away. At this point, the surface of the dielectric film is highly planarized since the profile of the sacrificial layer is transferred to the dielectric layer by the etchback procedure. The thickness of the dielectric film over underlying features, such as metal lines, may be thinner than desired after the etchback is completed. In some processes, in fact, the etchback step is allowed to proceed until the Metal-1 lines are exposed. In any case, an

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